

**Single Chip Wireless Sensor Node for *In-situ*  
Measurement of Selected Water Quality Parameters**

**By**

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the award of the

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## CANDIDATE'S DECLARATION

The work described in this thesis was carried by me under supervision of Prof. R.G.N. Meegama, Dr. M.K. Jayananda and Prof. M.M. Pathmalal and a report on this has not been submitted in whole or in part to any university or any other institution for another Degree/Diploma.



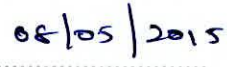
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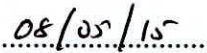
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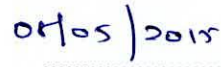


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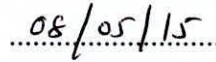
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# CONTENTS

<b>CANDIDATE'S DECLARATION</b>	<b>i</b>
<b>SUPERVISORS' RECOMMENDATION</b>	<b>ii</b>
<b>TABLE OF CONTENTS</b>	<b>iv</b>
<b>LIST OF FIGURES</b>	<b>viii</b>
<b>LIST OF TABLES</b>	<b>x</b>
<b>ABBREVIATIONS</b>	<b>xii</b>
<b>ACKNOWLEDGEMENT</b>	<b>xiii</b>
<b>ABSTRACT</b>	<b>xiv</b>
<b>1 INTRODUCTION</b>	<b>1</b>
1.1 Water Quality Standards . . . . .	2
1.2 Water Quality Parameters . . . . .	4
1.3 Present Water Quality Monitoring Methods . . . . .	5
1.3.1 Grab Sampling Method . . . . .	5
1.3.2 Automated and Continuous Monitoring Method . . . . .	6
1.3.3 Remote Sensing Method . . . . .	7
1.3.4 Using Sensitive Aquatic Organisms . . . . .	8
1.4 Importance of the Study . . . . .	8
1.5 Selected Water Quality Parameters . . . . .	9
1.5.1 pH Value . . . . .	9
1.5.2 Electrical Conductivity . . . . .	10
1.5.3 Dissolved Oxygen Level . . . . .	11
1.5.4 Water Temperature . . . . .	11
1.6 Research Problem . . . . .	13
1.7 Objectives of the Research . . . . .	15
1.8 Publications . . . . .	16
1.9 Structure of the Thesis . . . . .	17

<b>2</b>	<b>LITERATURE REVIEW</b>	<b>18</b>
2.1	Wireless Sensor Network Applications . . . . .	19
2.2	Key Challenge in Design of Wireless Sensor Nodes . . . . .	21
2.2.1	Power Efficiency . . . . .	22
2.2.2	Flexibility . . . . .	22
2.2.3	Robustness . . . . .	23
2.2.4	Communication . . . . .	23
2.2.5	Computation Power . . . . .	24
2.2.6	Size and Cost . . . . .	24
2.3	Existing Technologies and Standards . . . . .	25
2.3.1	Design of Computation Unit . . . . .	25
2.3.1.1	Microprocessors . . . . .	26
2.3.1.2	Micro-controllers . . . . .	27
2.3.1.3	Application Specific Integrated Circuits . . . . .	28
2.3.1.4	Field Programmable Gate Arrays . . . . .	29
2.3.1.5	Performance Evaluations . . . . .	31
2.4	Wireless Communication Protocols . . . . .	31
2.4.1	Wi-Fi . . . . .	32
2.4.2	Bluetooth . . . . .	32
2.4.3	ZigBee . . . . .	33
2.4.4	Cellular Networks . . . . .	34
2.4.5	Comparison Between the Communication Protocols . . . . .	36
2.5	IEEE1451 Standards . . . . .	37
2.5.1	Organization of the IEEE 1451 Family of Standards . . . . .	40
2.5.2	Benefits of using IEEE 1451 Smart Transducers for Interface to the Network . . . . .	47
2.6	Related Works . . . . .	48
<b>3</b>	<b>METHODOLOGY</b>	<b>62</b>
3.1	System Topology . . . . .	62
3.2	Design of Data Collecting Node . . . . .	65
3.2.1	Universal Asynchronous Receiver and Transmitter (UART) . . . . .	66
3.2.2	Receiver Circuit . . . . .	69
3.2.3	Receiver Buffer (Rx Buffer) . . . . .	72
3.2.4	Command Filter . . . . .	72
3.2.5	Transmission Buffer (Tx Buffer) . . . . .	73
3.2.6	Transmitter . . . . .	73
3.2.7	Baud Rate Generator . . . . .	73
3.2.8	Memory Block . . . . .	74
3.2.8.1	Transducer Electronic Data Sheet (TEDS) . . . . .	75

3.2.9	Transducer Controller . . . . .	78
3.2.10	Sensor Interface Blocks . . . . .	78
3.2.10.1	Analog-to-Digital (A to D) Interface Block . . . . .	78
3.2.10.2	One-wire interface block . . . . .	79
3.2.10.3	RS232 sensor interface . . . . .	88
3.2.11	Main Controller . . . . .	89
3.3	Design of Routing Node . . . . .	92
3.3.1	UART Interface . . . . .	93
3.3.2	Memory Block . . . . .	93
3.3.3	Main Controller . . . . .	93
3.3.4	Message Structures . . . . .	95
3.3.4.1	Inter-communication . . . . .	95
3.3.4.2	SMS messages . . . . .	98
3.4	Design of the Main Control Center . . . . .	99
3.5	Design of the Power Module . . . . .	100
<b>4</b>	<b>EXPERIMENTAL SETUP</b>	<b>102</b>
4.1	Data Collecting Node . . . . .	103
4.1.1	Sensor Array . . . . .	103
4.1.2	Interface sensors . . . . .	107
4.2	Memory Allocation . . . . .	109
4.2.1	Implementation of the TEDS's . . . . .	110
4.2.1.1	Meta TEDS . . . . .	110
4.2.1.2	Physical TEDS . . . . .	113
4.2.1.3	User's Transducer Name TEDS . . . . .	114
4.2.1.4	Transducer Channel TEDS . . . . .	115
4.2.2	Channel Enumeration . . . . .	117
4.2.3	Device Arrangement . . . . .	119
4.3	Routing Node . . . . .	121
4.3.1	Message Structures . . . . .	122
4.4	Communication Modules . . . . .	125
4.5	Main Control Center . . . . .	126
<b>5</b>	<b>RESULTS AND DISCUSSION</b>	<b>128</b>
5.1	Universal Asynchronous Receiver and Transmitter (UART) . . . . .	128
5.2	Sensor Array . . . . .	133
5.2.1	Temperature Sensor . . . . .	133
5.2.2	pH Sensor . . . . .	136
5.2.3	Electrical Conductivity Sensor . . . . .	139
5.2.4	Dissolved Oxygen Sensor . . . . .	141

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5.3	Evaluation of the Data Collecting Node . . . . .	142
5.4	System Testing . . . . .	147
<b>6</b>	<b>CONCLUSIONS</b>	<b>151</b>
	<b>Bibliography</b>	<b>154</b>



## LIST OF FIGURES

1.1	Distribution of earth's water . . . . .	2
2.1	The basic internal architecture of the FPGA chip . . . . .	29
2.2	(a) Conventional Transducer Model (b) IEEE 1451 smart transducer interface module with TEDS . . . . .	38
2.3	Context diagram of the IEEE 1451.2 interface specification . . . . .	41
2.4	Context diagram of the IEEE 1451.3 interface specification . . . . .	42
2.5	Context diagram of the IEEE 1451.5 interface specification . . . . .	43
2.6	Context diagram of the overall structure for the standards IEEE 1451 interface specification . . . . .	46
3.1	System Topology of the water quality monitoring system based on WSN .	63
3.2	Internal architecture of the data collecting node showing the functional blocks with inter-connectivity and transducer interfaces . . . . .	65
3.3	Internal architecture of the UART interface with functional blocks, flow of data and signals within the blocks and inputs/outputs to the interface .	66
3.4	Transmission of the UART data frame . . . . .	67
3.5	Optimal data extracting point of the data bit . . . . .	68
3.6	UART receive frame synchronization and data sampling points using the oversampling scheme . . . . .	69
3.7	State diagram of a UART receiver . . . . .	71
3.8	The internal memory organization of ROM that keeps TEDS and RAM holding sensor readings. . . . .	75
3.9	TEDS nested structure . . . . .	76
3.10	The internal architecture of a A to D interface block interface block . . . .	78
3.11	One-wire communication waveform for four basic operations: (a) write 1 bit, (b) write 0 bit, (c) read bit and (d) reset. . . . .	82
3.12	The functional steps of the 1-wire communication handled by the master device: . . . . .	86
3.13	Sub state diagram of the Reset(a), Write command(b) and Read command(c)	87
3.14	The internal architecture of a 1-wire interface block . . . . .	88
3.15	The Internal architecture of a RS232 interface block . . . . .	89
3.16	The overall operation of the data collecting node . . . . .	91
3.17	The internal architecture of the routing node . . . . .	92
3.18	The overall operation of the routing node . . . . .	94
3.19	The overall operation of the main control center . . . . .	100
3.20	Power module . . . . .	101
4.1	System Topology of the water quality monitoring system based on WSN .	103

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4.2	Atlas scientific pH kit: 1) pH probe,2) BNC connector, 3)pH circuit . . .	104
4.3	Atlas scientific dissolved oxygen kit : 1) DO probe,2) BNC connector, 3)DO circuit . . . . .	104
4.4	Atlas scientific electric conductivity kit: 1) EC probe,2) BNC connector, 3)EC circuit . . . . .	105
4.5	DS18B20 1-wire digital thermometer: 1) water proof DS18B20 temperature sensor, 2) pull-up resistor . . . . .	106
4.6	The internal architecture of a 1-wire interface block . . . . .	107
4.7	The Internal architecture of a RS232 interface block . . . . .	108
4.8	Physical appearance of the data collecting node . . . . .	119
4.9	Equipments arrangement of the data collecting node: 1)solar panel, 2) battery pack, 3) water proof DS18B20 temperature sensor, 4) DO probe, 5) pH probe, 6) EC probe, 7) EC circuit, 8) pH circuit, 9) DO circuit, 10) voltage controller unit, 11) power regulator unit, 12) switching circuit , 13) Zigbee module, 14) XESS XSA-3S1000 FPGA board . . . . .	120
4.10	Equipments arrangement of the routing node: 1) Xilinx XC3S1600E FPGA board, 2) GSM modem, 3)Xbee module . . . . .	121
4.11	"XBee-PRO" RF module . . . . .	125
4.12	TC35 GSM Module . . . . .	126
4.13	Map . . . . .	127
5.1	Actual temperature ranges measured using DS18B20 water-proof digital thermometer and sensION meter. . . . .	135
5.2	pH measurements taken from HQ40d meter and Atlas pH meter without proper calibration. . . . .	136
5.3	Estimated power consumption using several FPAG chips in the Sparten 3 family under different clock frequencies. . . . .	144
5.4	Curve of daily pH changes monitored by the system . . . . .	149
5.5	Curve of daily DO changes monitored by the system . . . . .	149
5.6	Curve of daily temperature changes monitored by the system . . . . .	150

## LIST OF TABLES

2.1	Compares the performance between the different implementation chips . . .	31
2.2	Comparison of the wireless protocols . . . . .	37
2.3	Summary of the IEEE 1451 family standards . . . . .	45
3.1	Steps of the procedures which followed by the receiver . . . . .	70
3.2	General format of the TEDS . . . . .	76
3.3	Importance of the mandatory TEDS . . . . .	77
3.4	Steps of the procedures which followed by the receiver . . . . .	81
3.5	Temperature and data relationship . . . . .	83
3.6	Functional steps which followed to collect temperature readings from the DS18B20 . . . . .	84
3.7	IEEE 1451 command message structure . . . . .	95
3.8	IEEE 1451 reply message structure . . . . .	96
3.9	Read TEDS Segment Command Structure . . . . .	97
3.10	TEDS Segment Command Reply Structure . . . . .	97
3.11	Read Transducer Channel data-set Segment reply argument . . . . .	98
3.12	Sample SMS message structure . . . . .	99
4.1	Specification of the selected sensors for data collecting node . . . . .	103
4.2	Three different types of conductivity sensors which can be connected to the E.C. circuit . . . . .	106
4.3	Memory allocation of the ROM memory block . . . . .	109
4.4	Memory allocation of the RAM memory block . . . . .	109
4.5	TEDS Identification . . . . .	111
4.6	Location definition of the UUID . . . . .	112
4.7	Meta TEDS . . . . .	113
4.8	Physical TEDS . . . . .	114
4.9	Radio type . . . . .	114
4.10	User's Transducer Name TEDS . . . . .	115
4.11	Transducer Channel TEDS . . . . .	116
4.12	Physical Units . . . . .	116
4.13	Sample definition . . . . .	117
4.14	Enumeration of the channels defined in the data collecting node . . . . .	118
4.15	Memory allocation of the ROM memory block . . . . .	122
4.16	Sample "wake up" request message . . . . .	122
4.17	Sample "read TEDS" request message . . . . .	123
4.18	Sample "read sensor values" request message . . . . .	123
4.19	Sample reply message for "read TEDS" command . . . . .	124

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4.20	Sample reply message for "read sensor values" command . . . . .	124
4.21	Sample SMS message . . . . .	124
5.1	Message loss percentage at different baud rates in practical conditions . .	131
5.2	Theoretical and experimental values obtained for the counter in the frequency divider . . . . .	132
5.3	Temperature readings taken from DS18B20 water-proof digital thermometer and sensION meter in water samples . . . . .	134
5.4	pH readings taken from HQ40d meter and Atlas pH meter at different dilutions . . . . .	138
5.5	EC readings taken from Weilheim meter and Atlas EC meter at different dilutions . . . . .	140
5.6	DO readings taken from HQ40d meter and Atlas pH meter at different dilutions . . . . .	142
5.7	Summary of device utilization as generated by the Xilinx tool . . . . .	143
5.8	Resources utilization and critical path delays in different FPGAs . . . . .	143
5.9	The intercept and gradient of selected FPGA chips . . . . .	145
5.10	Power consumption of the experimental setup . . . . .	146
5.11	Equipment cost of the experimental setup . . . . .	146
5.12	pH, DO and temperature readings collected using the monitoring system .	148

## ABBREVIATIONS

<b>ADC</b>	Analog-to-Digital
<b>ASCII</b>	American Standard Code for Information Interchange
<b>ASIC</b>	Application Specific Integrated Circuits
<b>CBL</b>	Configurable Logic Blocks
<b>DAC</b>	Digital-to-Analog
<b>DO</b>	Dissolved Oxygen
<b>EC</b>	Electric Conductivity
<b>FPGA</b>	Field Programmable Gate Arrays
<b>GSM</b>	Global System for Mobile Communications
<b>I/O</b>	Input and Output
<b>IEEE</b>	Institute of Electrical and Electronics Engineers
<b>MMI</b>	Mixed-Mode Interface
<b>NCAP</b>	Network Capable Application Processor
<b>RAM</b>	Random-access memory
<b>RF</b>	Radio Frequency
<b>ROM</b>	Read-only memory
<b>SMS</b>	Short Message Service
<b>STIM</b>	Smart Transducer Interface Module
<b>TBC</b>	Transducer Bus Controller
<b>TBIM</b>	Transducer Interface Bus Modules
<b>TDS</b>	Total Dissolved Solids
<b>TEDS</b>	Transducer Electronic Data Sheet
<b>TII</b>	Transducer Independent Interface
<b>TIM</b>	Transducer Interface Module
<b>UART</b>	Universal Asynchronous Receiver and Transmitter
<b>USB</b>	Universal Serial Bus
<b>WSN</b>	Wireless Sensor Network

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## ABSTRACT

The main focus of the work described in this thesis is to design a generalized, low cost re-configurable smart sensor node for wireless sensor network applications. Sensor nodes are designed using the single chip architecture which has embedding communication device handling, data processing, transducer control functionalities and Transducer Electronic Data Sheets (TEDS) in a single core.

FPGA (Field Programmable Gate Array) provides, re-programmable, re-configurable, high performance, flexibility etc. capabilities with consuming low power. Xilinx Spartan 3 FPGA family is selected as an implementation chip in this design. The Xilinx ISE Design Suite 14.1 is utilized as the developing tool with VHDL as the programming language.

IEEE 1451 family of standards defines a set of open, common, network-independent communication interfaces for connecting transducers (sensors or actuators) to the network and it defines the TEDS structure. IEEE 1451.0 and 1451.4 standards are followed for this implementation and TEDSs enable self-identification, self-diagnostics, self-description, location-awareness capabilities to the sensor node. As the proposed sensor node has these capabilities, it is referred to as a smart sensor node.

As Zigbee protocol is popular as a low cost and reliable method with advanced networking capabilities, Zigbee is selected to establish the communication between the sensor nodes.

The proposed node is evaluated under two methods such as performance measurements and reliability of the reading. Performance of the data collecting node is evaluated by using the results obtained by Xilinx tools and it confirms that the designed data collecting node can perform up to 52.802 MHz clock frequency in Xilinx Spartan 3 FPAG. In order to measure reliability of the readings, parameter values are collected by connecting sensors to it and results are compared with standard reference and statistically, there is no significant difference between the standard meter values and the values collected through the data collecting node.