Single Chip Wireless Sensor Node for *In-situ* Measurement of Selected Water Quality Parameters

By

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CANDIDATE'S DECLARATION

The work described in this thesis was carried by me under supervision of Prof. R.G.N. Meegama, Dr. M.K. Jayananda and Prof. M.M. Pathmalal and a report on this has not been submitted in whole or in part to any university or any other institution for another Degree/Diploma.

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SUPERVISORS' RECOMMENDATION

We certify that the above statement made by the candidate is true and that this thesis is suitable for submission to the University for the purpose of evaluation.

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ABBREVIATIONS

ADC	Analog-to-Digital
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuits
CBL	Configurable Logic Blocks
DAC	Digital-to-Analog
DO	Dissolved Oxygen
EC	Electric Conductivity
FPGA	Field Programmable Gate Arrays
GSM	Global System for Mobile Communications
I/O	Input and Output
IEEE	Institute of Electrical and Electronics Engineers
MMI	Mixed-Mode Interface
NCAP	Network Capable Application Processor
RAM	Random-access memory
RF	Radio Frequency
ROM	Read-only memory
SMS	Short Message Service
STIM	Smart Transducer Interface Module
TBC	Transducer Bus Controller
TBIM	Transducer Interface Bus Modules
TDS	Total Dissolved Solids
TEDS	Transducer Electronic Data Sheet
TII	Transducer Independent Interface
TIM	Transducer Interface Module
UART	Universal Asynchronous Receiver and Transmitter
USB	Universal Serial Bus
WSN	Wireless Sensor Network

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ABSTRACT

The main focus of the work described in this thesis is to design a generalized, low cost re-configurable smart sensor node for wireless sensor network applications. Sensor nodes are designed using the single chip architecture which has embedding communication device handling, data processing, transducer control functionalities and Transducer Electronic Data Sheets (TEDS) in a single core.

FPGA (Field Programmable Gate Array) provides, re-programmable, re-configurable, high performance, flexibility etc. capabilities with consuming low power. Xilinx Spartan 3 FPGA family is selected as an implementation chip in this design. The Xilinx ISE Design Suite 14.1 is utilized as the developing tool with VHDL as the programming language.

IEEE 1451 family of standards defines a set of open, common, network-independent communication interfaces for connecting transducers (sensors or actuators) to the network and it defines the TEDS structure. IEEE 1451.0 and 1451.4 standards are followed for this implementation and TEDSs enable self- identification, self-diagnostics, self-description, location-awareness capabilities to the sensor node. As the proposed sensor node has these capabilities, it is referred to as a smart sensor node.

As Zigbee protocol is popular as a low cost and reliable method with advanced networking capabilities, Zigbee is selected to establish the communication between the sensor nodes.

The proposed node is evaluated under two methods such as performance measurements and reliability of the reading. Performance of the data collecting node is evaluated by using the results obtained by Xilinx tools and it confirms that the designed data collecting node can perform up to 52.802 MHz clock frequency in Xilinx Sparten 3 FPAG. In order to measure reliability of the readings, parameter values are collected by connecting sensors to it and results are compared with standard reference and statistically, there is no significant difference between the standard meter values and the values collected through the data collecting node.